What Is Claimed Is:

1. A circuit to screen for defects in an addressable line in a non-volatile memory array, said circuit comprising:

a current mirror circuit connected to the addressable line and having a plurality of mirroring stages; said current mirror circuit for receiving a control signal, and mirroring said control signal to provide a current to said addressable line;

wherein said current on said addressable line is used to screen for defects.

2. The circuit of claim 1 wherein one of said plurality of mirroring stages is connected to said addressable line and to a source of high voltage.

3. The circuit of claim 2 wherein one of said plurality of mirroring stages for receiving the control signal comprises:

a first MOS transistor having a first threshold voltage;

a second MOS transistor having a second threshold voltage;

wherein said first and second MOS transistors are connected in parallel with the gate of said first and second MOS transistors connected together for receiving the control signal;

wherein said first threshold voltage is lower than said second threshold voltage; and

wherein said first MOS transistor is a weaker transistor than said second MOS transistor.

4. The circuit of claim 3 wherein said second MOS transistor is connected in series to a diode connected NMOS transistor.

5. A method of screening for defects in an addressable line in a non-volatile memory array, said method comprising:

supplying a control signal to a current mirror circuit connected to the addressable line;

mirroring said control signal by the current mirror circuit to provide a current to the addressable line;

using said current to screen for defects on said addressable line.

6. The method of claim 5 wherein said current mirror circuit supplies a current from a high voltage source to the addressable line.

7. The method of claim 6 wherein said addressable line has a length having a first end and a second end, and wherein said current is supplied substantially near the first end, and wherein the using step comprises:

measuring for current flow substantially near the second end, wherein the current flow measured is indicative of potential defects on the addressable line.

8. The method of claim 6 wherein said addressable line has a plurality of non-volatile memory cells electrically connected thereto, and wherein the current from the current mirror circuit can change the state of the cells; and wherein the using step comprises:

reading the state or the memory cells connected to the addressable line to determine if the state of the cells were changed.

9. The method of claim 6 wherein said addressable line is a word line.